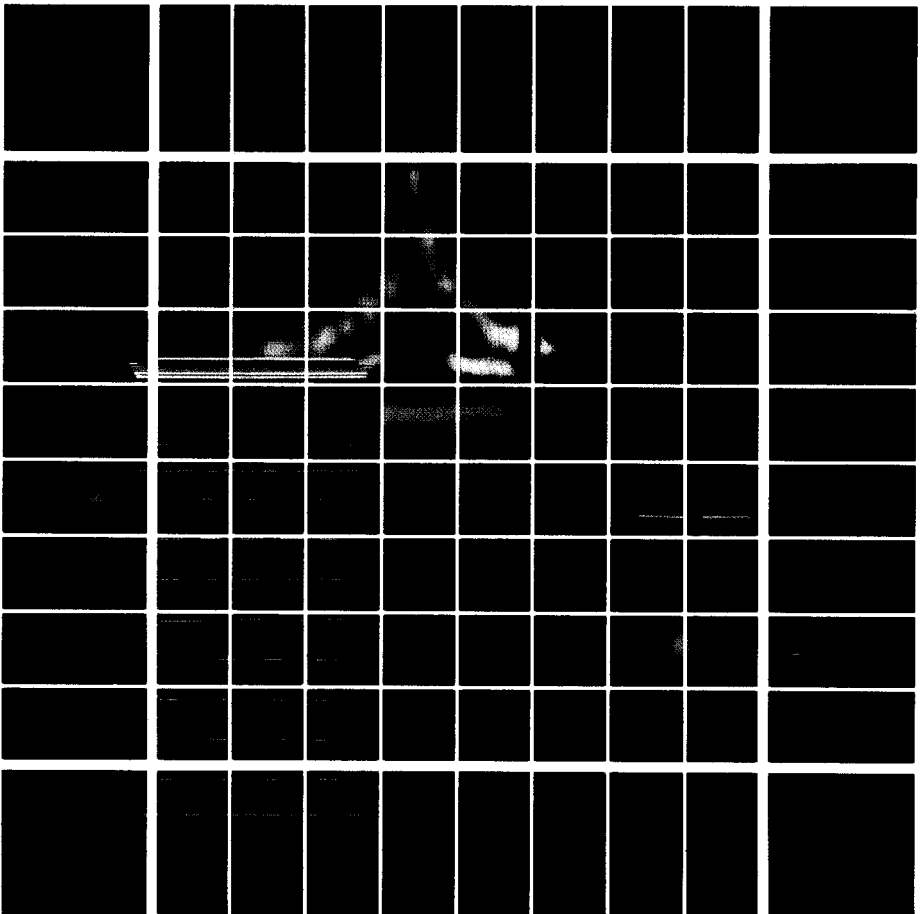


HEWLETT-PACKARD

HP-41C

CIRCUIT  
ANALYSIS PAC



## **NOTICE**

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## INTRODUCTION

The Circuit Analysis Pac consists of a general network analysis program, GNAP, and a ladder network analysis program, LNAP. This manual provides a description of each program, relevant equations, a set of instructions for using the programs, and several example problems, each of which includes a list of keystrokes required for its solution.

Before plugging in your Application Module, turn the calculator off, and be sure you understand the section "Inserting and Removing Application Modules." Before using a particular program, take a few minutes to read "Format of User Instructions" and "A Word About Program Usage."

You should first familiarize yourself with a program by running it once or twice following the user instructions in the manual. Thereafter, the program's prompting or the mnemonics on the overlays should provide the necessary instructions, including which variables are to be input, which keys are to be pressed, and which values will be output.

We hope that the Circuit Analysis Pac will assist you in the solution of numerous problems. As you become familiar with your Pac, please feel free to send us your comments and suggestions about this Pac or about other solutions programs you would like to see. Send your comments and suggestions to:

Hewlett-Packard  
Corvallis Division Customer Support  
1000 N.E. Circle Blvd.  
Corvallis, OR 97330, U.S.A.

If you have technical problems with this Pac or with the HP-41, consult your owner's handbook.

### Note:


Application modules are designed to be used in both HP-41C and HP-41CV model calculators. The HP-41C and HP-41CV differ only in their initial Continuous Memory capacities. The term "HP-41C" is used throughout the rest of this manual, unless otherwise specified, to refer to both calculators.

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## INSERTING AND REMOVING APPLICATION MODULES

Before you insert an Application Module for the first time, familiarize yourself with the following information.

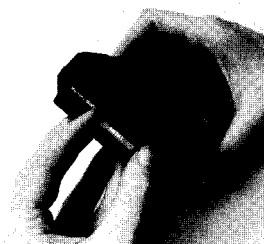
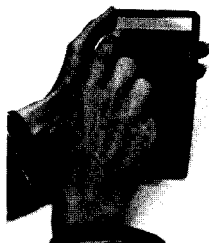
Up to four Application Modules can be plugged into the ports on the HP-41C. While plugged in, the names of all programs contained in the Module can be displayed by pressing  **CATALOG** 2.

### CAUTION

Always turn the HP-41C off before inserting or removing any plug-in extension or accessories. Failure to turn the HP-41C off could damage both the calculator and the accessory.

To insert Application Modules:

1. Turn the HP-41C off! Failure to turn the calculator off could damage both the Module and the calculator.
2. Remove the port covers. Remember to save the port covers; they should be inserted into the empty ports when no extensions are inserted.
3. Insert the Application Module with the label facing downward as shown, into any port **after** the last Memory Module. For example, if you have a Memory Module inserted in port 1, you can insert an Application Module in any of ports 2, 3, or 4. (The port numbers are shown on the back of the calculator.) **Never insert an Application Module into a lower numbered port than a Memory Module.**



#### 4 Inserting and Removing Application Modules

4. If you have additional Application Modules to insert, plug them into any port after the last Memory Module. Be sure to place port covers over unused ports.
5. Turn the calculator on and follow the instructions given in this book for the desired application functions.

To remove Application Modules:

1. Turn the HP-41C off! Failure to do so could damage both the calculator and the Module.
2. Grasp the desired Module handle and pull it out as shown.



3. Place a port cap into the empty ports.

#### **Mixing Memory Modules and Application Modules**

Any optional accessories (such as the HP-82104A Card Reader, or the HP-82143A Printer) should be treated in the same manner as Application Modules. That is, they can be plugged into any port after the last Memory Module. Also, the HP-41C should be turned off prior to insertion or removal of these extensions.

The HP-41C allows you to leave gaps in the port sequence when mixing Memory and Application Modules. For example, you can plug a Memory Module into port 1 and an Application Module into port 4, leaving ports 2 and 3 empty.

## FORMAT OF USER INSTRUCTIONS

The completed User Instruction Form— which accompanies each program is your guide to operating the programs in this Pac.

The form is composed of five labeled columns. Reading from left to right, the first column, labeled STEP, gives the instruction step number.

The INSTRUCTIONS column gives instructions and comments concerning the operations to be performed.

The INPUT column specifies the input data, the units of data if applicable, or the appropriate alpha response to a prompted question. Data input keys consist of 0 to 9 and the decimal point (the numeric keys), **EEX** (enter exponent), and **CHS** (change sign).

The FUNCTION column specifies the keys to be pressed after keying in the corresponding input data.

The DISPLAY column specifies prompts, intermediate and final answers, and their units, where applicable.

Above the DISPLAY column is a box which specifies the minimum number of data storage registers necessary to execute the program. Refer to the Owner's Handbook for information on how the SIZE function affects storage configuration.

The following illustrates the User Instruction Form for the GNAP program.

				<b>SIZE &gt; 40</b>
STEP	INSTRUCTIONS	INPUT	FUNCTION	DISPLAY
1	Initialize the GNAP program		<b>XEQ</b> GNAP <b>R/S</b> <sup>2</sup>	GNAP NODES= ?
2	Key in: number of nodes number of branches	N B	<b>R/S</b> <b>R/S</b> <b>R/S</b> <sup>2</sup>	BRANCHES= ? N= (N)B= (B) <sup>1</sup> BRANCH 1
3	Key in each branch element: a) Resistance (Ohms)  or b) Capacitance (Farads)  or c) Inductance (Henrys)  and enter branch nodes or d) Transconductance (Siemens)	R  C  L  FR. TO  gm	<b>A</b>  <b>B</b>  <b>C</b>  <b>R/S</b>  <b>D</b>	NODES: FR. TO= ?  NODES: FR. TO= ?  NODES: FR. TO= ? BRANCH(n+ 1)  INPUT: V+ .V- = ?

## A WORD ABOUT PROGRAM USAGE

### Catalog

When an Application Module is plugged into a port of the HP-41C, the contents of the Module can be reviewed by pressing **■ CATALOG** 2 (the Extension Catalog). Executing the **■ CATALOG** function lists the name of each program or function in the Module, as well as functions of any other extensions which might be plugged in.

### Overlays

Overlays have been included for some of the programs in this Pac. To run the program, choose the appropriate overlay, and place it on the calculator. The mnemonics on the overlay are provided to help you run the program. The program's name is given vertically on the left side. When the calculator is in USER mode, a blue mnemonic identifies the key directly above it. Gold mnemonics are similar to blue mnemonics, except that they are above the appropriate key and the shift (gold) key must be pressed before the re-defined key. Once again, USER mode must be set.

### ALPHA and USER Mode Notation

This manual uses a special notation to signify ALPHA mode. Whenever a statement on the User Instruction Form is printed in gold, the **■ ALPHA** key must be pressed before the statement can be keyed in. After the statement is input, press **■ ALPHA** again to return the calculator to its normal operating mode, or to begin program execution. For example, **■ XEQ** GNAP means press the following keys: **■ XEQ** **■ ALPHA** GNAP **■ ALPHA** .

When the calculator is in USER mode, this manual will use the symbols **■ A** - **■ J** and **■ A** - **■ E** to refer to the reassigned keys in the top two rows. These key designations will appear on the User Instruction Form and in the keystroke solutions to sample problems.

### Optional HP-82143A Printer

When the optional printer is plugged into the HP-41C along with the Circuit Analysis Application Module, all results will be printed automatically. You may also want to keep a permanent record of the values input to a certain program. A convenient way to do this is to set the Print Mode switch to NORMAL before running the program. In this mode, all input values and the corresponding keystrokes will be listed on the printer, thus providing a record of the entire operation of the program.

### Using Programs as Subroutines

The programs in this Pac may be called as subroutines for user programs in the HP-41C's program memory. Refer to Appendix B for information on special subroutine calling points.



## Downloading Module Programs

If you wish to trace execution, to modify, or to record on magnetic cards a program in this Application Module, it must first be copied into the HP-41C's program memory. For information concerning the HP-41C's COPY function, see the Owner's Handbook. It is not necessary to copy a program in order to run it.

## Program Interruption

These programs have been designed to operate properly when run from beginning to end, without turning the calculator off (remember, the calculator may turn itself off). If the HP-41C is turned off, it may be necessary to set flag 21 (SF 21) to continue proper execution.

## Use of Labels

You should generally avoid writing programs into the calculator memory that use program labels identical to those in your Application Module. In case of a label conflict, the label within program memory has priority over the label within the Application Pac program.

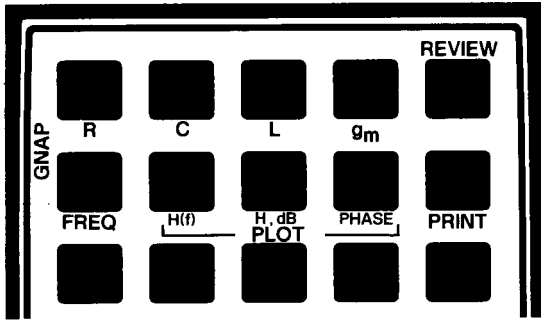
Several labels used in the Circuit Analysis Module are also used in other modules. If you have this module and another plugged into your calculator, you should make sure that the module containing the programs you want to use is in the lower numbered port.

You will find a list of all the global labels used in this Application Module at the back of the manual in appendix C, Program Labels. The names of modules or accessories where duplicate labels occur are also listed. Before plugging in two or more modules, check that listing for duplicate label conflicts.

## Assigning Program Names

Key assignments to keys **A** - **J** and **A** - **E** take priority over the automatic assignments of local labels in the Application Module. Be sure to clear previously assigned functions before executing a Module program.

# GENERAL NETWORK ANALYSIS PROGRAM



This program analyzes electrical networks, computing amplitude and phase of the transfer function  $V_2(s)/V_1(s)$ . If the optional HP-82143A printer is used, the results may be either printed or plotted. The network elements allowed are resistors, capacitors, inductors, and voltage-controlled current sources. The size of the circuit that can be handled by the program depends on the number of memory registers available. The following table indicates the number of nodes,  $N$ , and branches,  $B$ , that can be analyzed with three memory modules. The number of registers needed for a circuit is  $2N^2 + 3B + 29$ .

## POSSIBLE CIRCUIT CONFIGURATIONS

### Number of Memory Modules

0		1		2		3	
N	B	N	B	N	B	N	B
2	8	2	30	2	51	2	72
3	5	3	26	3	48	3	69
		4	22	4	43	4	64
		5	16	5	37	5	58
		6	8	6	30	6	51
				7	21	7	42
				8	11	8	32
						9	21

Assuming you have set the minimum size of 28, the GNAP program begins by asking you for the size of your circuit and then tests to determine if there is enough storage before it begins. If there is insufficient storage, the message "SET SIZE NNN" warns you that the number of data registers must be increased. When numbering the nodes in your circuit, be sure that node 0 is ground, node 1 is the input node, and node 2 is the node whose voltage you wish to determine.

**Analysis Algorithm**

For any network, a matrix called the “nodal admittance matrix” can be written.\* This matrix gives the relationship between the node voltages and the branch currents:

$$Y_n V_n = A I \tag{1}$$

where:

- A is the incidence matrix
- V<sub>n</sub> is the node-voltage vector
- I is the source-current vector
- Y<sub>n</sub> is the nodal admittance matrix

The algorithm assumes that our network is driven only by a current source of 1 ampere flowing from the ground node, node 0, into the input node, node 1. Equation (1) can then be written as

$$Y_n V_n = \begin{bmatrix} 1 \\ 0 \\ 0 \\ \cdot \\ \cdot \\ \cdot \end{bmatrix} \tag{2}$$

This equation could be solved explicitly for each node voltage by multiplying both sides on the left by Y<sub>n</sub><sup>-1</sup>.

$$V_n = Y_n^{-1} \begin{bmatrix} 1 \\ 0 \\ 0 \\ \cdot \\ \cdot \\ \cdot \end{bmatrix} \tag{3}$$

But since we only need the ratio V<sub>2</sub>/V<sub>1</sub>, it is not necessary to invert Y<sub>n</sub>. Instead, we can use Gaussian elimination to transform Y<sub>n</sub> into a lower triangular matrix.

$$\begin{bmatrix} a_{11} & 0 & 0 & 0 & \dots & \dots & \dots \\ a_{21} & a_{22} & 0 & 0 & \dots & \dots & \dots \\ a_{31} & a_{32} & a_{33} & 0 & \dots & \dots & \dots \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ a_{n1} & a_{n2} & a_{n3} & \dots & \dots & \dots & a_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ \cdot \\ \cdot \\ \cdot \\ V_n \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ \cdot \\ \cdot \\ \cdot \\ 0 \end{bmatrix} \tag{4}$$

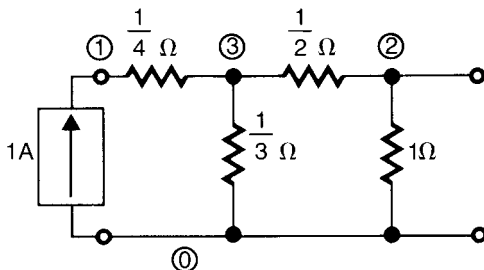
\*See Balabanian & Bickart, *Electrical Network Theory*, Wiley, New York, 1969 or equivalent.

## 10 General Network Analysis Program

Then we compute the desired ratio by solving the second equation, obtained from (4).

$$\frac{V_2}{V_1} = -\frac{a_{21}}{a_{22}} \quad (5)$$

To illustrate this procedure, consider this circuit:



By using the techniques of Sec. 2.4 of Balabanian, we can write the  $Y_n$  matrix

$$Y_n = \begin{bmatrix} 4 & 0 & -4 \\ 0 & 3 & -2 \\ -4 & -2 & 9 \end{bmatrix}$$

Multiplying the third row by  $\frac{2}{9}$  and adding it to the second, we get

$$Y_n = \begin{bmatrix} 4 & 0 & -4 \\ -\frac{8}{9} & \frac{23}{9} & 0 \\ -4 & -2 & 9 \end{bmatrix}$$

Since we don't need to triangularize past the second row, we have

$$\frac{V_2}{V_1} = \frac{8}{23} = -9.17 \text{ dB}$$

For circuits containing reactive components, the above procedure is carried out in the same way except that all operations are done with complex numbers. The GNAP program works with a real conductance matrix,  $G$ , and an imaginary susceptance matrix,  $B$ .

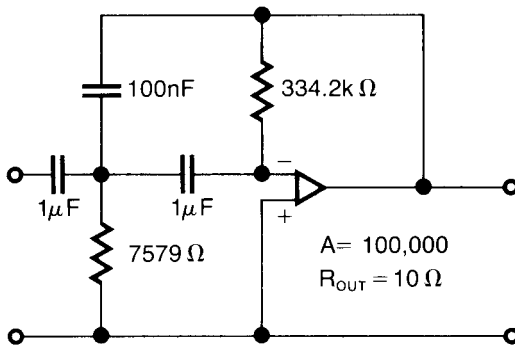
You might get the message DATA ERROR if there is a resonant subnetwork in your circuit and the frequency being used is the exact resonant frequency. If this condition occurs, it will be necessary to alter your input frequency slightly.

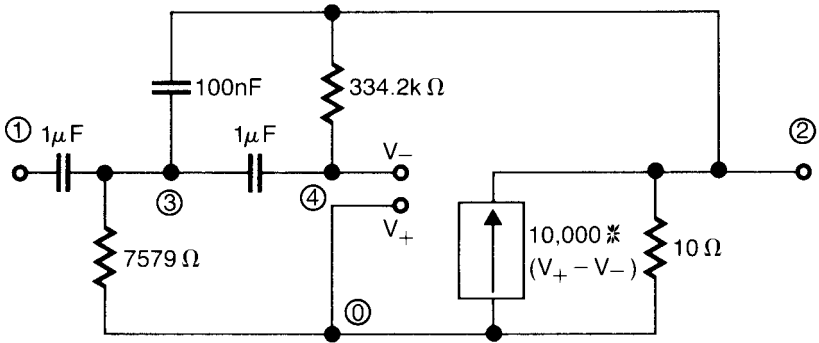
				SIZE > 40
STEP	INSTRUCTIONS	INPUT	FUNCTION	DISPLAY
1	Initialize the GNAP program		<input type="checkbox"/> XEQ GNAP <input type="checkbox"/> R/S <sup>2</sup>	GNAP NODES=?
2	Key in: number of nodes number of branches	N B	<input type="checkbox"/> R/S <input type="checkbox"/> R/S <input type="checkbox"/> R/S <sup>2</sup>	BRANCHES=? N=(N)B=(B) <sup>1</sup> BRANCH 1
3	Key in each branch element: a) Resistance (Ohms)  or b) Capacitance (Farads)  or c) Inductance (Henrys)  and enter branch nodes <sup>3</sup> or d) Transconductance (Siemens)  and enter voltage control  and current nodes (current leaves . current enters) Repeat step 3 for all branches. When done with all,	R  C  L  FR. TO  gm  V+ .V-  IL.IE	<input type="checkbox"/> A  <input type="checkbox"/> B  <input type="checkbox"/> C  <input type="checkbox"/> R/S  <input type="checkbox"/> D  <input type="checkbox"/> R/S  <input type="checkbox"/> R/S	NODES: FR. TO=? NODES: FR. TO=? NODES: FR. TO=? BRANCH(n+1)  INPUT: V+ .V-=? OUTPUT: IL.IE=?  BRANCH (n+1)
4	(OPTIONAL) To review the circuit:		<input type="checkbox"/> E <input type="checkbox"/> R/S <sup>2</sup> : :	DONE BRANCH 1 (List of Input) : :
5	Specify the frequency sweep: Key in: Lowest Frequency Highest Frequency frequency increment <sup>4</sup>	f <sub>MIN</sub> f <sub>MAX</sub> Δf	<input type="checkbox"/> F <input type="checkbox"/> R/S <input type="checkbox"/> R/S <input type="checkbox"/> R/S	FMIN=? FMAX=? F INCR=? READY
6	To compute and list results: Press <input type="checkbox"/> R/S until results have been obtained for all frequencies.  <sup>1</sup> If SET SIZE NNN appears, you need more data registers. Set SIZE as indicated and continue by pressing <input type="checkbox"/> R/S .  <sup>2</sup> If you are using the printer these Run/Stops are not required.  <sup>3</sup> The grounded NODE of a passive branch must be the TO node.  <sup>4</sup> If Δf is entered as a negative value, the program uses Δ as a multiplicative increment.		<input type="checkbox"/> J <input type="checkbox"/> R/S <sup>2</sup> <input type="checkbox"/> R/S <sup>2</sup> <input type="checkbox"/> R/S <sup>2</sup> : :	frequency magnitude magnitude,dB phase : :

STEP	INSTRUCTIONS	INPUT	FUNCTION	DISPLAY
7	To plot the results (assuming you have an HP-82143A printer attached), select desired plot: a) magnitude or b) magnitude in dB or c) Phase		<input type="checkbox"/> G <input type="checkbox"/> H <input type="checkbox"/> I	YMIN=? YMIN=? YMIN=?
8	Specify plot parameters: Key in a) $Y_{MIN}$ b) $Y_{MAX}$ c) x-axis (y-intercept)	$Y_{MIN}$ $Y_{MAX}$ x-axis <sup>5</sup>	<input type="checkbox"/> R/S <input type="checkbox"/> R/S <input type="checkbox"/> R/S	YMAX=? AXIS=?
	<p><sup>5</sup>You may suppress printing of the x-axis by placing any alpha character in the alpha display, e.g.: <input type="checkbox"/> ALPHA NO AXIS <input type="checkbox"/> R/S causes "NO AXIS" to be stored as the y-intercept and no axis will be plotted.</p>			

**Example 1:**

Compute the magnitude and phase response for this active filter. It was designed to be a high-pass filter with a 10-Hz cutoff frequency, passband gain of 20 dB, and  $\alpha$ -peaking factor of 1.





**Keystrokes**

**XEQ ALPHA** SIZE **ALPHA** 082  
**XEQ ALPHA** GNAP **ALPHA**

**R/S**  
 4 **R/S**  
 7 **R/S**  
**R/S**  
 1 **EEX CHS** 6 **B**  
 1.03 **R/S**  
 7579 **A**  
 3 **R/S**  
 1 **EEX CHS** 6 **B**  
 3.04 **R/S**  
 100 **EEX CHS** 9 **B**  
 3.02 **R/S**  
 334200 **A**  
 4.02 **R/S**  
 10000 **D**  
 .04 **R/S**  
 .02 **R/S**  
 10 **A**  
 2 **R/S**  
**F**  
 1 **R/S**  
 100 **R/S**  
 10 **USER**  $\sqrt{x}$  **USER** **CHS** **R/S**

**Display**

**GNAP**

**NODES?**  
**BRANCHES?**  
**N=4 B=7**  
**BRANCH 1**  
**NODES: FR.TO=?**  
**BRANCH 2**  
**NODES: FR.TO=?**  
**BRANCH 3**  
**NODES: FR.TO=?**  
**BRANCH 4**  
**NODES: FR.TO=?**  
**BRANCH 5**  
**NODES: FR.TO=?**  
**BRANCH 6**  
**INPUT: V+.V-=?**  
**OUTPUT: IL.IE=?**  
**BRANCH 7**  
**NODES: FR.TO=?**  
**DONE**  
**FMIN=?**  
**FMAX=?**  
**F INCR=?**  
**READY**

These keystrokes assume the printer is not being used.

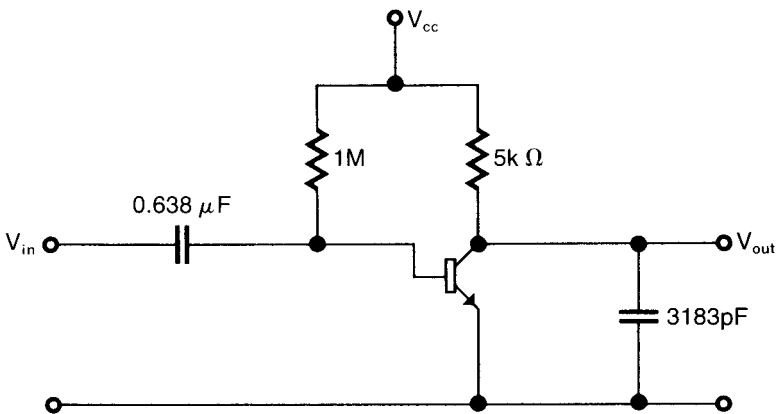
**Keystrokes**

**Display**

<b>J</b>	<b><math>F=1.00</math></b>
<b>R/S</b>	<b><math>H=0.10</math></b>
<b>R/S</b>	<b><math>H=-19.96dB</math></b>
<b>R/S</b>	<b><math>L=-5.77</math></b>
<b>R/S</b>	<b><math>F=3.16</math></b>
<b>R/S</b>	<b><math>H=1.05</math></b>
<b>R/S</b>	<b><math>H=0.41dB</math></b>
<b>R/S</b>	<b><math>L=-19.36</math></b>
<b>R/S</b>	<b><math>F=10.00</math></b>
<b>R/S</b>	<b><math>H=10.00</math></b>
<b>R/S</b>	<b><math>H=20.00dB</math></b>
<b>R/S</b>	<b><math>L=-90.00</math></b>
<b>R/S</b>	<b><math>F=31.62</math></b>
<b>R/S</b>	<b><math>H=10.48</math></b>
<b>R/S</b>	<b><math>H=20.41dB</math></b>
<b>R/S</b>	<b><math>L=-160.64</math></b>
<b>R/S</b>	<b><math>F=100.00</math></b>
<b>R/S</b>	<b><math>H=10.05</math></b>
<b>R/S</b>	<b><math>H=20.04dB</math></b>
<b>R/S</b>	<b><math>L=-174.23</math></b>

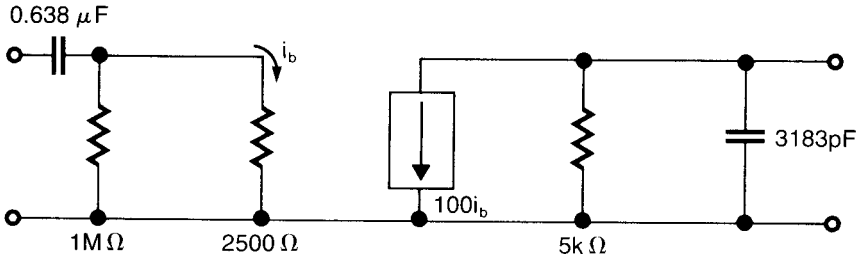
**Example 2:**

Create a Bode plot for this transistor amplifier.

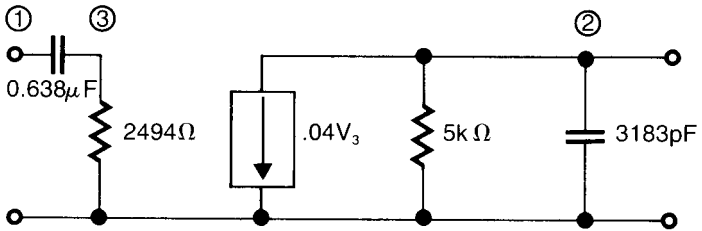




First transform the circuit using an h-parameter model.



Then replace the current-controlled current source with a voltage-controlled current source.



**Keystrokes**

XEQ ALPHA SIZE ALPHA 062  
 XEQ ALPHA GNAP ALPHA  
 3 R/S  
 5 R/S  
 .638 EEX CHS 6 B  
 1.03 R/S  
 2494 A  
 3 R/S  
 .04 D  
 3 R/S  
 2 R/S  
 5000 A  
 2 R/S  
 3183 EEX CHS 12 B  
 2 R/S  
 E

**Display**

GNAP  
 NODES?  
 BRANCHES?  
 N=3 B=5  
 BRANCH 1  
 NODES: FR.TO=?  
 BRANCH 2  
 NODES: FR.TO=?  
 BRANCH 3  
 INPUT: V+.V-=?  
 OUTPUT:IL.IE=?  
 BRANCH 4  
 NODES: FR.TO=?  
 BRANCH 5  
 NODES: FR.TO=?  
 DONE  
 B 1.  
 C=638.0E-9  
 NODES: 1.0300  
 B 2.  
 R=2.494E3  
 NODES: 3.0000

These key-strokes assume a printer is being used.

Review the circuit description

**Keystrokes**

[F]  
 10 [R/S]  
 1 [EEX] 5 [R/S]  
 10 [USER] [√x] [√x] [USER] [CHS] [R/S]  
 [H]  
 20 [R/S]  
 50 [R/S]  
 50 [R/S]

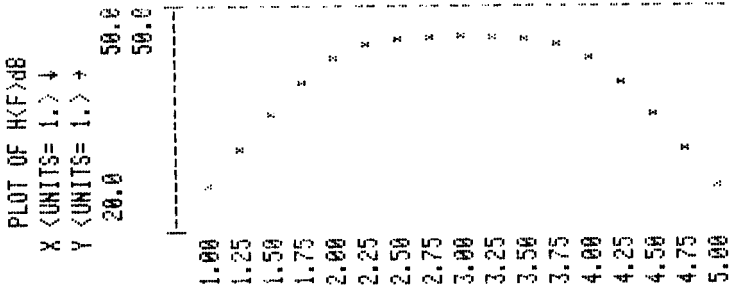
**Display**

**B 3.**  
**GM= 40.00E-3**  
**NODES: 300.0200 (V+ V- .ILIE)**

**B 4.**  
**R= 5.000E3**  
**NODES: 2.0000**

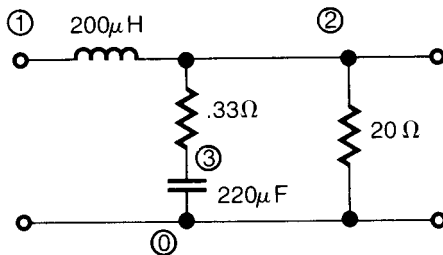
**B 5.**  
**C= 3.183E-9**  
**NODES: 2.0000**  
**FMIN=?**  
**FMAX=?**  
**F INCR =?**  
**READY**  
**YMIN=?**  
**YMAX=?**  
**AXIS=?**

Four steps per decade.



**Example 3:**

Analyze this circuit from 100 Hz to 100 kHz. Make Bode plots using a multiplicative frequency increment of  $10^{1/4}$ .



**Keystrokes**

**XEQ** **ALPHA** SIZE **ALPHA** 059

**XEQ** **ALPHA** GNAP **ALPHA**

3 **R/S**

4 **R/S**

200 **EEX** **CHS** 6 **C**

1.02 **R/S**

.33 **A**

2.03 **R/S**

220 **EEX** **CHS** 6 **B**

3 **R/S**

20 **A**

2 **R/S**

**F**

100 **R/S**

1 **EEX** 5 **R/S**

10 **USER** **√x** **√x** **√x** **USER** **CHS**

**R/S**

**H** (**J** if you have no printer)

50 **CHS** **R/S**

10 **R/S**

0 **R/S**

**Display**

**GNAP**

**NODES?**

**BRANCHES?**

**N=3 B=4**

**BRANCH 1**

**NODES: FR.TO=?**

**BRANCH 2**

**NODES: FR.TO=?**

**BRANCH 3**

**NODES: FR.TO=?**

**BRANCH 4**

**NODES: FR.TO=?**

**DONE**

**FMIN=?**

**FMAX=?**

**F INCR = ?**

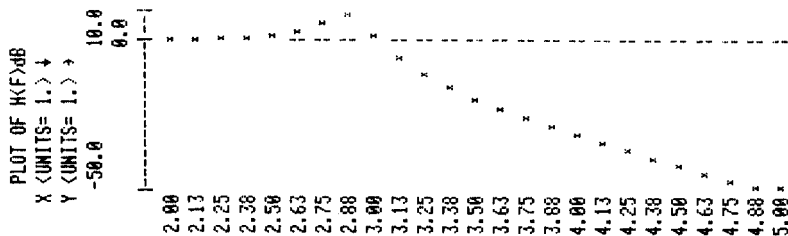
**READY**

**YMIN=?**

**YMAX=?**

**AXIS=?**

If SIZE > 59,  
ignore this line.  
These keystrokes  
assume a printer  
is being used.

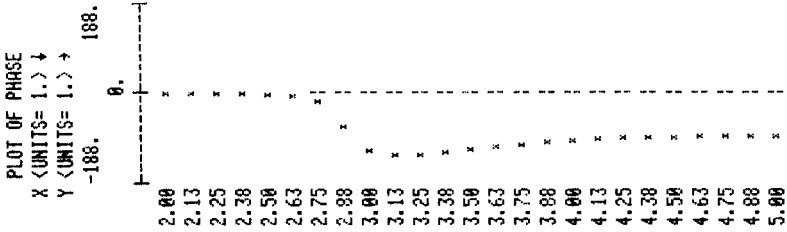


**Keystrokes**

**Display**

**I**  
 188 **CHS** **R/S**  
 188 **R/S**  
 0 **R/S**

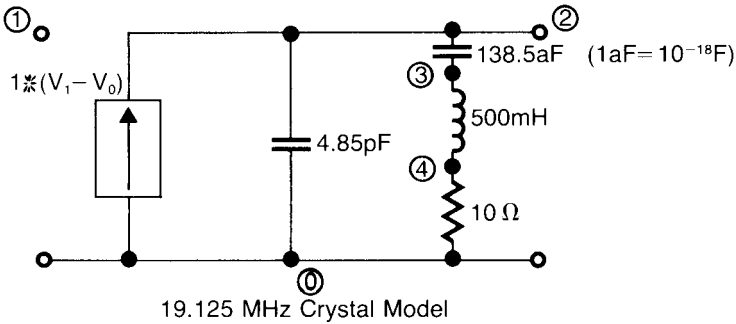
**YMIN=?**  
**YMAX=?**  
**AXIS=?**



**Example 4:**

You can use programs of your own to put any desired label on a plot. Store Ymin, Ymax, Axis, and the Label. Then execute PRPLOTP.

This example shows how to use a Voltage-Controlled Current Source to determine the input impedance of a circuit and how to plot it with the label "Z IN."



First build the circuit.

**Keystrokes**

**Display**

**XEQ** **ALPHA** SIZE **ALPHA** 076  
**XEQ** **ALPHA** GNAP **ALPHA**

4 **R/S**

5 **R/S**

1 **D**

**GNAP**  
**NODES?**  
**BRANCHES?**  
**N=4 B=5**  
**BRANCH 1**  
**INPUT: V+.V-=?**

These key-strokes assume the printer is being used.

**Keystrokes**

1 **R/S**  
 .02 **R/S**  
 4.85 **EEX** **CHS** 12 **B**  
 2 **R/S**  
 138.5 **EEX** **CHS** 18 **B**  
 2.03 **R/S**  
 500 **EEX** **CHS** 3 **C**  
 3.04 **R/S**  
 10 **A**  
 4 **R/S**  
**F**  
 19125300 **R/S**  
 19125800 **R/S**  
 50 **R/S**

Then write this short program.

**Keystrokes**

**■** **GTO** **•** **•**  
**PRGM**  
**■** **LBL** **ALPHA** Z IN **ALPHA**  
**■** **GTO** **ALPHA** H<F> **ALPHA**  
**PRGM**  
 0 **STO** 00  
 50000 **STO** 01  
**ALPHA** Z IN **■** **STO** 04  
**■** **STO** 11 **ALPHA**  
**XEQ** **ALPHA** PRPLOT **ALPHA**

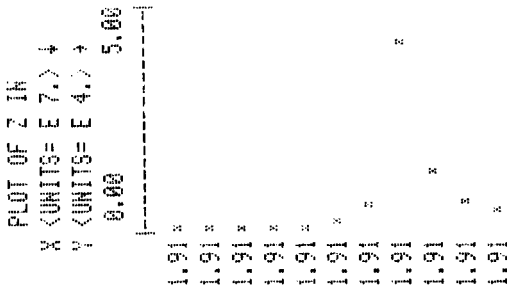
**Display**

**OUTPUT:IL,IE=?**  
**BRANCH 2**  
**NODES: FR.TO=?**  
**BRANCH 3**  
**NODES: FR.TO=?**  
**BRANCH 4**  
**NODES: FR.TO=?**  
**BRANCH 5**  
**NODES: FR.TO=?**  
**DONE**  
**FMIN=?**  
**FMAX=?**  
**F INCR=?**  
**READY**

**Display**

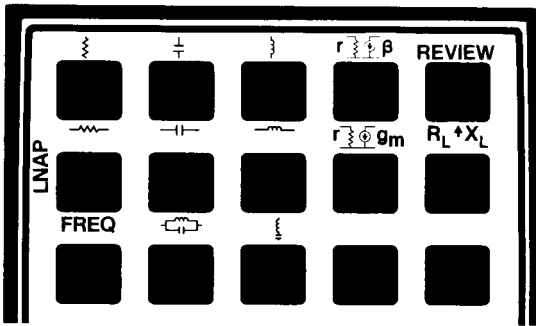
**PACKING**  
**01 LBL Z IN**  
**02 GTO H<F>**

Ymin\*  
 Ymax  
 No Axis  
 Name



\*For a description of the function PRPLOT and the registers used to store its plot parameters, see your **Printer Owner's Handbook**.

## LADDER NETWORK ANALYSIS PROGRAM



This program analyzes ladder networks of up to 107 branches providing amplitude and phase of various transfer functions, either printed or plotted. Network elements allowed are resistors, capacitors, inductors, series and parallel inductor-capacitor combinations, voltage-controlled current sources, current-controlled current sources, transformers, gyrators, transmission lines, open stub lines, and shorted stub lines. Transfer functions computed are  $V_2/V_1$ ,  $I_2/I_1$ ,  $P_2/P_1$  and  $Z_{in}$ .

Network size is determined by the number of memory modules present. The maximum number of branches possible is 107.

Memory Modules	Branches (maximum)
0	11
1	43
2	75
3	107

If SIZE is not large enough, the display will show "NONEXISTENT." You may execute SIZE with a larger argument and then press **[R/S]** to resume execution of the program. You need at least  $40 + 2 \times (\text{number of elements})$  data registers to run this program. Some elements require three storage registers.

### Theoretical Basis of Ladder Network Analysis Program

The operation of this program is based on the fact that the chain-parameter matrix of two cascaded circuits is equal to the product of their individual chain-parameter matrices. Circuit elements are stored as they are input from left to right. Then at each frequency the individual chain-parameter matrices are formed and multiplied to gradually compute the overall matrix. Finally, the desired transfer function is computed.

The chain-parameter matrix is defined by the following sketch and matrix equation.  $\Psi$  is the Cyrillic letter "cha".



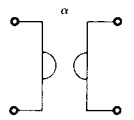
$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \Psi_{11} & \Psi_{12} \\ \Psi_{21} & \Psi_{22} \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

The circuit elements allowed by this program are shown below with their  $\Psi$ -matrices.

Name	Circuit	Chain-Parameter Matrix
RS Series Resistor		$\Psi = \begin{bmatrix} 1/\Omega & R/\Omega \\ 0 & 1/\Omega \end{bmatrix}$
RP Parallel Resistor		$\Psi = \begin{bmatrix} 1/\Omega & 0 \\ \frac{1}{R} \Omega & 1/\Omega \end{bmatrix}$
CS Series Capacitor		$\Psi = \begin{bmatrix} 1/\Omega & \frac{1}{\omega C} \angle -90^\circ \\ 0 & 1/\Omega \end{bmatrix}$
CP Parallel Capacitor		$\Psi = \begin{bmatrix} 1/\Omega & 0 \\ \omega C \angle 90^\circ & 1/\Omega \end{bmatrix}$
LS Series Inductor		$\Psi = \begin{bmatrix} 1/\Omega & \omega L \angle 90^\circ \\ 0 & 1/\Omega \end{bmatrix}$
LP Parallel Inductor		$\Psi = \begin{bmatrix} 1/\Omega & 0 \\ \frac{1}{\omega L} \angle -90^\circ & 1/\Omega \end{bmatrix}$
LCS Series L-C		$\Psi = \begin{bmatrix} 1/\Omega & \frac{\omega L}{1 - \omega^2 LC} \angle 90^\circ \\ 0 & 1/\Omega \end{bmatrix}$
LCP Parallel L-C		$\Psi = \begin{bmatrix} 1/\Omega & 0 \\ \frac{\omega C}{1 - \omega^2 LC} \angle 90^\circ & 1/\Omega \end{bmatrix}$
TF Transformer		$\Psi = \begin{bmatrix} n/\Omega & 0 \\ 0 & \frac{1}{n} \Omega \end{bmatrix}$

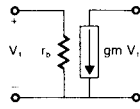
## 22 Ladder Network Analysis Program

GY Gyrator



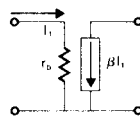
$$\mathbf{q} = \begin{bmatrix} 0 & \alpha L0 \\ \frac{1}{\alpha} L0 & 0 \end{bmatrix}$$

VCIS Voltage-Controlled Current Source



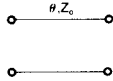
$$\mathbf{q} = \begin{bmatrix} 0 & -\frac{1}{g_m} L0 \\ 0 & -\frac{1}{r_b g_m} L0 \end{bmatrix}$$

ICIS Current-Controlled Current Source



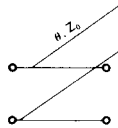
$$\mathbf{q} = \begin{bmatrix} 0 & -\frac{r_b}{\beta} L0 \\ 0 & -\frac{1}{\beta} L0 \end{bmatrix}$$

LINE Transmission Line



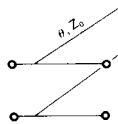
$$\mathbf{q} = \begin{bmatrix} \cos\theta L0 & Z_0 \sin\theta L90 \\ \frac{\sin\theta}{Z_0} L90 & \cos\theta L0 \end{bmatrix}$$

STUBO Open Stub



$$\mathbf{q} = \begin{bmatrix} 1L0 & 0 \\ \frac{\tan\theta}{Z_0} L90 & 1L0 \end{bmatrix}$$

STUBS Shorted Stub



$$\mathbf{q} = \begin{bmatrix} 1L0 & 0 \\ \frac{\cot\theta}{Z_0} L-90 & 1L0 \end{bmatrix}$$

Any of the following transfer functions may be computed from the overall chain-parameter matrix.

Input impedance

$$|Z_{in}| = \frac{q_{11} Z_L + q_{12}}{q_{21} Z_L + q_{22}}$$

Power Gain

$$\left| \frac{P_{out}}{P_{in}} \right| = \left| \frac{I_2}{I_1} \right|^2 \frac{\text{Re}\{Z_L\}}{\text{Re}\{Z_{in}\}}$$

Voltage transfer ratio

$$\left| \frac{V_2}{V_1} \right| = \frac{Z_L}{q_{11} Z_L + q_{12}}$$

Forward transfer admittance

$$\left| \frac{I_2}{V_1} \right| = \frac{-1}{q_{11} Z_L + q_{12}}$$

Current transfer ratio

$$\left| \frac{I_2}{I_1} \right| = \frac{-1}{q_{21} Z_L + q_{22}}$$

Forward transfer impedance

$$\left| \frac{V_2}{I_1} \right| = \frac{Z_L}{q_{21} Z_L + q_{22}}$$

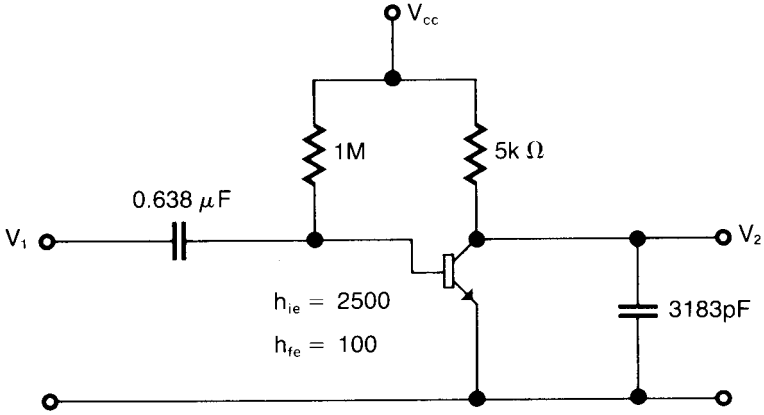


				SIZE > 50
STEP	INSTRUCTIONS	INPUT	FUNCTION	DISPLAY
1	Initialize the Ladder Network Analysis Program		<b>XEQ</b> LNAP <b>R/S</b> *	LNAP BEGIN INPUT
2	Input circuit elements one at a time starting at the left.			
	Series Resistor	R	<b>A</b>	RS= (R)
	Parallel Resistor	R	<b>A</b>	RP= (R)
	Series Capacitor	C	<b>B</b>	CS= (C)
	Parallel Capacitor	C	<b>B</b>	CP= (C)
	Series Inductor	L	<b>C</b>	LS= (L)
	Parallel Inductor	L	<b>C</b>	LP= (L)
	Voltage-Controlled Current Source	r g <sub>m</sub>	<b>ENTER</b> * <b>D</b>	VCIS= (r), (g <sub>m</sub> )
	Current-Controlled Current Source	r β	<b>ENTER</b> * <b>D</b>	ICIS= (r), (β)
	Series L-C	L C	<b>ENTER</b> * <b>G</b>	LCS= (L), (C)
	Parallel L-C	L C	<b>ENTER</b> * <b>H</b>	LCP= (L), (C)
	Transformer	n	<b>XEQ</b> TF	TF= (n)
	Gyator	α	<b>XEQ</b> GY	GY= (α)
	Transmission Line ( $\theta = \frac{\text{electrical length}}{f_0}$ )	θ Z <sub>o</sub>	<b>ENTER</b> * <b>XEQ</b> LINE	LINE= (θ), (Z <sub>o</sub> )
	Open Stub	θ Z <sub>o</sub>	<b>ENTER</b> * <b>XEQ</b> STUBO	STUBO= (θ), (Z <sub>o</sub> )
	Shorted Stub	θ Z <sub>o</sub>	<b>ENTER</b> * <b>XEQ</b> STUBS	STUBS= (θ), (Z <sub>o</sub> )
3	Input load impedance:	R <sub>L</sub> X <sub>L</sub>	<b>ENTER</b> * <b>E</b>	
4	(Optional) Review the circuit. Press <b>R/S</b> to see successive branches.  *This <b>R/S</b> is not needed if you are using a printer.		<b>E</b>	

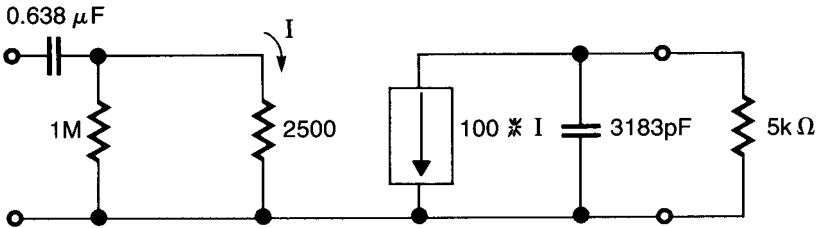
STEP	INSTRUCTIONS	INPUT	FUNCTION	DISPLAY
5	Select frequency sweep Minimum frequency Maximum frequency Frequency increment (negative value indicates multiplicative increment)	$f_{\text{MIN}}$ $f_{\text{MAX}}$  $\Delta f$	[F] [R/S] [R/S]  [R/S]	FMIN=? FMAX=? FINCR=?  FUNCTION?
6	To output results, key in a list-function name. (The calculator is already in ALPHA mode.) Transfer voltage ratio Transfer current ratio Power ratio Input Impedance All of the above	V2/V1 I2/I1 P2/P1* ZIN ALL	[R/S] [R/S] [R/S] [R/S] [R/S]	
7	To plot results, key in the desired plot-function name. (The calculator is already in ALPHA mode.) Plot Magnitude of V2/V1 Plot Magnitude of V2/V1 in dB Plot Angle of V2/V1  Plot Magnitude of I2/I1 Plot Magnitude of I2/I1 in dB Plot Angle of I2/I1  Plot Magnitude of ZIN Plot Angle of ZIN		PV PVdB P/V  PI PIdB P/LI  PZIN PLZIN	YMIN=? YMIN=? YMIN=?  YMIN=? YMIN=? YMIN=?  YMIN=? YMIN=?
8	Specify plotting information  (Any alpha-data input yields no axis)	$Y_{\text{MIN}}$ $Y_{\text{MAX}}$  axis	[R/S] [R/S]  [R/S]	YMAX=? AXIS=?
9	When the plot is complete, you may return to step 1, step 3, or step 5. If you wish to return to step 6, press		[J]	FUNCTION?
	*This is the <b>real</b> power ratio as only the real portions of $Z_L$ and $Z_{in}$ are considered.			

**Example 1:**

Make Bode plots (magnitude and phase) of  $V_2/V_1$  for this transistor amplifier.



Transform the circuit using an h-parameter model.



**Keystrokes**

```

[ ] [FIX] 2
[XEQ] [ALPHA] SIZE [ALPHA] 051
[XEQ] [ALPHA] LNAP [ALPHA]
[R/S]
.638 [EEX] [CHS] 6 [B]
1 [EEX] 6 [ ] [A]
2500 [ENTER+] 100 [ ] [D]
3183 [EEX] [CHS] 12 [ ] [B]
5000 [ENTER+] 0 [E]
[F]
10 [R/S]
100000 [R/S]
10 [USER] [sqrt] [sqrt] [USER] [CHS] [R/S]
    
```

**Display**

```

LNAP
BEGIN INPUT
CS=6.38E-7
RP=1,000,000.00
ICIS=2,500.00,100.00
CP=3.18E-9
ZL=5,000.00+J0.00
FMIN = ?
FMAX = ?
FINCR = ?
FUNCTION?
    
```

PVdB (R/S)

20 (R/S)

50 (R/S)

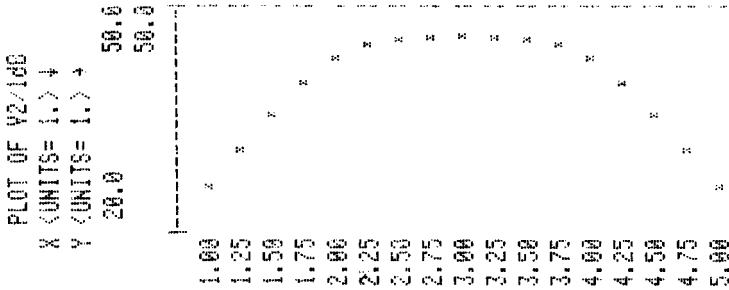
50 (R/S)

YMIN = ?

YMAX = ?

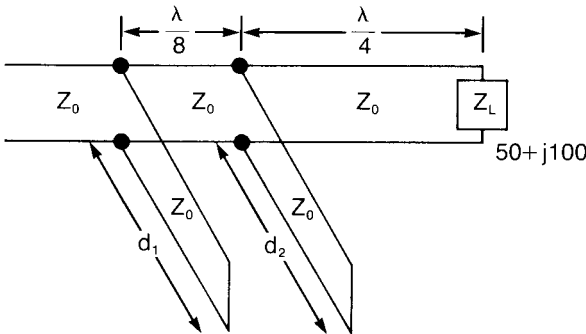
AXIS = ?

If you have no printer, V2/V1 (R/S) will cause individual values to be output.



**Example 2:**

If the stub lengths,  $d_1$  and  $d_2$ , are  $54^\circ$  and  $49.68^\circ$  respectively, what is the input impedance of this double-stub tuner? ( $Z_0$  is  $100\Omega$ )



**Keystrokes**

(FIX) 2  
 (XEQ) (ALPHA) SIZE (ALPHA) 053  
 (XEQ) (ALPHA) LNAP (ALPHA)  
 (R/S)  
 54 (ENTER+)  
 100 (XEQ) (ALPHA) STUBS (ALPHA)  
 45 (ENTER+)  
 100 (XEQ) (ALPHA) LINE (ALPHA)  
 49.68 (ENTER+)

**Display**

LNAP  
BEGIN INPUT

STUBS=54.00,100.00  
LINE=45.00,100.00

You might like to assign STUBS to a key, say  (xzy) .

**Keystrokes**

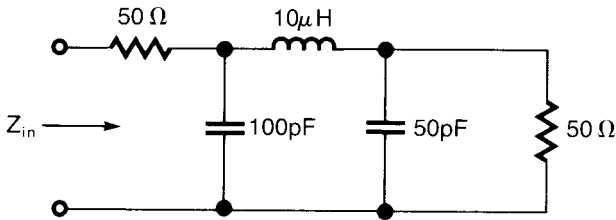
100 **XEQ** **ALPHA** STUBS **ALPHA**  
 90 **ENTER**  
 100 **XEQ** **ALPHA** LINE **ALPHA**  
 50 **ENTER** 100 **E**  
**F**  
 1 **R/S**  
**R/S**  
**R/S**  
 ZIN **R/S**  
**R/S**  
**R/S**  
**R/S**  
**R/S**

**Display**

**STUBS=49.68,100.00**  
**LINE=90.00,100.00**  
**ZL=50.00+J100.00**  
**FMIN = ?**  
**FMAX = ?**  
**FINCR = ?**  
**FUNCTION?**  
**F=1.00**  
**ZIN=97.00**  
**L-1.27**  
**ZIN = 96.97**  
**+J - 2.15**

**Example 3:**

What is the input impedance of the circuit shown at 1 MHz and 10 MHz?



**Keystrokes**

**FIX** 0  
**XEQ** **ALPHA** SIZE **ALPHA** 048  
**XEQ** **ALPHA** LNAP **ALPHA**  
**R/S**  
 50 **A**  
 100 **EEX** **CHS** 12 **B**  
 10 **EEX** **CHS** 6 **C**  
 50 **EEX** **CHS** 12 **B**  
 50 **ENTER** 0 **E**

**Display**

**LNAP**  
**BEGIN INPUT**  
**RS=50.**  
**CP=1.E-10**  
**LS=1.E-5**  
**CP=5.E-11**  
**ZL=50.+J0.**

## Keystrokes

**F**  
 1 **EEX** 6 **R/S**  
 10 **EEX** 6 **R/S**  
 9 **EEX** 6 **R/S**  
 ZIN **R/S**  
**R/S**  
**R/S**  
**R/S**  
**R/S**  
**R/S**  
**R/S**  
**R/S**  
**R/S**  
**R/S**

## Display

**FMIN = ?**  
**FMAX = ?**  
**FINCR = ?**  
**FUNCTION?**  
**F= 1,000,000.**  
**ZIN= 122.**  
**∠31.**  
**ZIN= 104.**  
**+J63.**  
**F= 10,000,000.**  
**ZIN= 221.**  
**∠-75.**  
**ZIN= 56.**  
**+J- 213.**

**PROGRAM DATA**

Program	# Regs. to Copy	Data Registers	Flags
GNAP	195		
	00	Ymin	05 S: $\Delta f$ is multiplicative
	01	Ymax	C: $\Delta f$ is additive
	02	PRPLOT scratch	06 S: Node is ground
	03	Plotting Character	07 S: Plot dB
	04	Axis	08 S: Plot phase
	05	PRPLOT scratch	09 S: Plot magnitude
	06	f	
	07	scaling multiplier	
	08	fmin	
	09	fmax	
	10	$\Delta f$	
	11	Plot Name	
	12		
	13	number of freqs	
	14	J K	
	15	MJ V+ JK	
	16	MM V- JJ	
	17	IJ IL KJ	
	18	IM IE KK	
	19	I J	
	20	M.002	
	21	28+ 3b	
	22	maximum V2/V1	
	23	component-type pointer	
	24	component-value pointer	

25	branches, b nodes, n
26	
27	
28	
27+b	Component types
28+b	
27+3b	Component values and nodes
28+3b	
28+3b+n <sup>2</sup>	G matrix (Re{Y})
27+3b+2n <sup>2</sup>	B matrix (Im{Y})

Program	# Regs. to Copy	Data Registers	Flags
LNAP	283	Ymin	5 S: $\Delta f$ is multiplicative
		Ymax	C: $\Delta f$ is additive
		PRPlot scratch	6 S: Don't print frequency
		Plotting character	C: Print frequency
		Axis	7 S: Plot magnitude in dB



8 S: Plot phase  
 9 S: Plot magnitude  
 10 S: Don't increment f  
 20 S: Always execute  
 \* AN  
 C: Execute \* AN  
 only once

05 PRPlot scratch  
 06 f  
 07 Scaling multiplier  
 08 fmin  
 09 fmax  
 10 f  
 11 Plot Name  
 12 Re {Y<sub>11</sub>}  
 13 Im {Y<sub>12</sub>}  
 14 Re {Y<sub>12</sub>}  
 15 Im {Y<sub>12</sub>}  
 16 Re {Y<sub>21</sub>}  
 17 Im {Y<sub>21</sub>}  
 18 Re {Y<sub>22</sub>}  
 19 Im {Y<sub>22</sub>}  
 20 Re {A}  
 21 Im {A}  
 22 Re {B}  
 23 Im {B}  
 24 Re {C}  
 25 Im {C}  
 26 Re {D}  
 27 Im {D}  
 28 Re {temporary}

29	Im {temporary}
30	Pointer to next element
31	Number of elements, n
32	RL
33	XL
34	Re $\{ Y_{11}Z_L + Y_{12} \}$
35	Im $\{ Y_{11}Z_L + Y_{12} \}$
36	Re $\{ Y_{21}Z_L + Y_{22} \}$
37	Im $\{ Y_{21}Z_L + Y_{22} \}$
38	not used
39	not used
40	List of network elements and values
45	. . . . . .

## SUBROUTINES

This table provides information necessary to use various portions of the Circuit Analysis Application Module as subroutines.

SUBROUTINE	LABEL	INITIAL REGISTERS	FLAG STATUS	FINAL REGISTERS	REMARKS
Complex Multiply	*C*	t:V <sub>2</sub> z:U <sub>2</sub> y:V <sub>1</sub> x:U <sub>1</sub>		y: Im{(U <sub>1</sub> + iV <sub>1</sub> ) (U <sub>2</sub> + iV <sub>2</sub> )} x: Re{(U <sub>1</sub> + iV <sub>1</sub> ) (U <sub>2</sub> + iV <sub>2</sub> )}	
Complex Add	*C+	t:V <sub>2</sub> z:U <sub>2</sub> y:V <sub>1</sub> x:U <sub>1</sub>		y: V <sub>1</sub> + V <sub>2</sub> x: U <sub>1</sub> + U <sub>2</sub>	
GNAP PRINT	*J		See Appendix A for detailed information regarding register contents and flag settings.		This label is provided so that a user-level program can initiate a GNAP analysis after the user has initially set up the circuit.

APPENDIX C  
PROGRAM LABELS

Label	Duplicate Label In
*J	Home Management Pac
PV	Home Management Pac Real Estate Pac
RS	Petroleum Fluids Pac
*AN      LINE      P/V *C*      LINE=      RP *C+      LCP      RP= *MAT*    LCP=      RS= ALL      LCS      R= CP      LCS=      STUBS CP=      LNAP      STUBS= CS      LP      STUBO CS=      LP=      STUBO= C=      LS      TF GM=      LS=      TF= GNAP      L=      VCIS GY      PHASE    VCIS= GY=      PI      V2/V1 H<F>    PldB      V2/1dB H<F>dB   PP2/P1    /V2/V1 ICIS      PVdB      /I2/I1 ICIS=      PZIN      /ZIN I2/I1      P2/P1 I2/1dB    P/I	No Label Conflicts

The labels in this list are not in the same order as they appear in the catalog listing for the module.



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